IN THE CLAIMS

1. (canceled)

2. (currently amended) A control circuit for configuring at least one I/O module connector pin, said circuit comprising:

~~at least one port~~a processor controlling a configuration of the at least ~~one pin,~~one pin via at least one port, wherein one of said at least one port ~~comprises at least~~is configured to be one of a Pull-Down (PD) port, a Pull-Up (PU) port, a Discrete High (DH) port, a Discrete Low (DL) port, a positive 15 volt (P15V) port, a negative 15 volt (N15V) port, a range (RANGE) port, and a voltage out (VOUT) port; and

a comparator configured to provide an output to a processor located within said ~~circuit.~~circuit, wherein an input of said comparator is coupled to a plurality of switch assemblies including switches and voltage supplies, said switch assemblies configured to operate said at least one pin in one of a plurality of modes.

3. (currently amended) A control circuit for configuring at least one I/O module connector pin, said circuit comprising:

~~at least one port~~a processor controlling a configuration of the at least ~~one pin;~~one pin via at least one port;

~~at least one switch assembly~~a plurality of switch assemblies comprising ~~a solid state switch,~~a plurality of solid state switches, said ~~at least one port~~processor controlling whether a respective solid state switch of said ~~at least one~~ solid state ~~switch~~switches is in an open state or a closed state; and

a comparator configured to provide an output to ~~a processor located within said circuit.~~said processor, wherein an input of said comparator is coupled to said switch assemblies including said solid state switches and voltage supplies, said switch assemblies configured to operate said at least one pin in one of a plurality of modes.

4. (currently amended) A control circuit in accordance with Claim 3 wherein ~~the at least one switch assembly comprises at least~~one of said solid state switches is configured to

be one of a Pull-Down switch, a Pull-Up switch, a Discrete High switch, a Discrete Low switch, a positive 15 volt switch, a negative 15 volt switch, a range switch, and a voltage out switch.

5. (currently amended) A control circuit in accordance with Claim 3 ~~wherein the~~wherein said processor determines a configuration of one of the ~~at least one switch assembly determines the configuration of the at least one pin.~~switch assemblies.

6. (canceled)

7. (currently amended) An I/O module comprising:

at least one connector pin;

a control circuit comprising a plurality of solid state switches, said solid state switches ~~controlling~~being operated to control a configuration of the at least one pin; and

a comparator configured to provide an output to a processor located within said ~~circuit.~~circuit, wherein an input of said comparator is coupled to a plurality of switch assemblies including said solid state switches and voltage supplies, said switch assemblies configured to operate said at least one pin in one of a plurality of modes.

8. (currently amended) An I/O module in accordance with Claim 7 wherein said ~~circuit further comprising at least one port controlling~~processor controls a configuration of a respective at least one switch.

9. (currently amended) An I/O module in accordance with Claim 8 wherein said processor controls an energization state of ~~each said~~ at least one port located within said processor, said processor controlling a state of a respective at least one ~~switch.~~switch by controlling the energization state of each said at least one port.

10. (currently amended) An I/O module in accordance with Claim 8 wherein said processor includes at least one port and one of said at least one port ~~comprises at least~~is configured to be one of a Pull-Down (PD) port, a Pull-Up (PU) port, a Discrete High (DH) port, a Discrete Low (DL) port, a positive 15 volt (P15V) port, a negative 15 volt (N15V) port, a range (RANGE) port, and a voltage out (VOUT) port.

11. (currently amended) An I/O module in accordance with Claim 7 wherein one of said switches ~~comprising at least~~is configured to be one of a Pull-Down switch, a Pull-Up switch, a Discrete High switch, a Discrete Low switch, a positive 15 volt switch, a negative 15 volt switch, a range switch, and a voltage out switch.

12. (canceled)

13. (currently amended) A PLC comprising:

an I/O module comprising at least one connector pin and a control circuit comprising a plurality of ports, a configuration of the at least one connector pin determined by ~~an energization state of~~a processor including said ports;

a comparator configured to provide an output to ~~a processor~~said processor located within said ~~circuit; and~~circuit, wherein an input of said comparator is coupled to a plurality of switch assemblies including switches and voltage supplies, said switch assemblies configured to operate said at least one connector pin in one of a plurality of modes; and

a CPU coupled to said I/O module.

14. (currently amended) A PLC in accordance with Claim 13 wherein one of said ~~at least one port comprises at least one of~~ports is configured to be a Pull-Down (PD) port, a Pull-Up (PU) port, a Discrete High (DH) port, a Discrete Low (DL) port, a positive 15 volt (P15V) port, a negative 15 volt (N15V) port, a range (RANGE) port, and a voltage out (VOUT) port.

15. (currently amended) A PLC in accordance with Claim 13 ~~further comprising at least one switch assembly comprising a switch,~~ wherein said ~~at least one port~~processor controlling whether ~~a respective said at least one switch~~one of said switches is in an open state or a closed state.

16. (currently amended) A PLC in accordance with Claim 15 wherein ~~the at least one switch assembly comprises at least~~one of said switches is configured to be one of a Pull-Down switch, a Pull-Up switch, a Discrete High switch, a Discrete Low switch, a positive 15 volt switch, a negative 15 volt switch, a range switch, and a voltage out switch.

17. (currently amended) A PLC in accordance with Claim 15 wherein ~~the configuration of the at least one switch assembly determines the configuration of said at least one connector pin.~~said processor determines a configuration of one of the switches.

18. (canceled)

19. (currently amended) A method for configuring at least one connector pin utilizing a control circuit, the control circuit including at least one port, said method comprising:

providing an energization state to the at least one port;

controlling a configuration of the at least one connector pin by utilizing ~~the energization state of~~a processor including the at least one ~~port; and~~port;

providing an output from a comparator to ~~a processor~~the processor located within the control ~~circuit.~~circuit; and

coupling an input of the comparator to a plurality of switch assemblies including switches and voltage supplies, the switch assemblies configured to operate the at least one connector pin in one of a plurality of modes.

20. (currently amended) A method in accordance with Claim 19 wherein one of the at least one port ~~comprises at least~~is configured to be one of a Pull-Down (PD) port, a Pull-Up (PU) port, a Discrete High (DH) port, a Discrete Low (DL) port, a positive 15 volt (P15V) port, a negative 15 volt (N15V) port, a range (RANGE) port, and a voltage out (VOUT) port.

21. (currently amended) A method in accordance with ~~Claim 19 wherein the control circuit includes at least one switch assembly including a switch,~~Claim 19, said method further comprising:

utilizing the energization state of the at least one port to control whether ~~a respective at least one switch~~one of the switches is in an open state or a closed state; and

controlling a configuration of the at least one connector pin by utilizing ~~the state~~one of the open and closed states of ~~the at least one switch.~~one of the switches.

22. (currently amended) A method in accordance with Claim 21 wherein one of the ~~at least one switch assembly includes at least~~switches is configured to be one of a Pull-Down switch, a Pull-Up switch, a Discrete High switch, a Discrete Low switch, a positive 15 volt switch, a negative 15 volt switch, a range switch, and a voltage out switch.

23. (canceled)

24. (currently amended) An I/O module comprising:

at least one connector pin;

a control circuit comprising:

~~a plurality of switches controlling a configuration of said at least one pin and at least one port controlling a configuration of a respective at least one switch, an energization state of each said at least one port controlling a state of a respective at least one switch; and~~a processor controlling a configuration of said at least one connector pin by operating a plurality of switches; and

a comparator configured to provide an output to ~~a processor~~said processor located within said ~~circuit.~~circuit, wherein an input of said comparator is coupled to a plurality of switch assemblies including said switches and voltage supplies, said switch assemblies configured to operate said at least one connector pin in one of a plurality of modes.

25. (currently amended) An I/O module comprising:

at least one connector ~~pin; and~~pin;

a control circuit comprising a processor that operates a plurality of switches ~~controlling~~to control a configuration of said at least one pin, ~~said circuit utilizing a single DAC for each said connector pin to implement~~wherein the configuration is one of a twenty-four volt positive logic discrete input mode, a twenty-four volt negative logic discrete input mode, a twenty-four volt high side discrete output mode without open wire detection, a twenty-four volt high side discrete output mode with open wire detection, zero volt low side discrete output mode without open wire detection, a zero volt low side discrete output mode

with open wire detection, zero to ten volt analog input mode, and a zero to ten volt analog output mode; and

a comparator configured to provide an output to ~~a processor located within~~ said ~~circuit.~~processor, wherein a first input of said comparator is coupled to a plurality of switch assemblies including said switches and voltage supplies, a second input of said comparator coupled to a digital to analog converter that receives a reference signal from said processor, said switch assemblies configured to operate said at least one connector pin in one of a plurality of modes.

26. (currently amended) An I/O module in accordance with Claim 25 wherein ~~said circuit further comprising at least one port controlling~~to operate said switches said processor controls a configuration of a respective at least one switch.

27. (canceled)

28. (currently amended) A method for configuring at least one connector pin utilizing a control circuit, said method comprising:

controlling a configuration of the at least one connector ~~pin utilizing a single DAC for each pin of the at least one connector pin to implement~~pin, wherein the configuration is one of a twenty-four volt positive logic discrete input mode, a twenty-four volt negative logic discrete input mode, a twenty-four volt high side discrete output mode without open wire detection, a twenty-four volt high side discrete output mode with open wire detection, a zero volt low side discrete output mode without open wire detection, a zero volt low side discrete output mode with open wire detection, a zero to ten volt analog input mode, and a zero to ten volt analog output ~~mode; and~~mode;

providing an output from a comparator to a processor located within the control ~~circuit.~~circuit;

coupling a first input of the comparator to a plurality of switch assemblies including a plurality of switches and voltage supplies, the switch assemblies configured to operate the at least one connector pin in one of a plurality of modes; and

coupling a second input of the comparator to a digital to analog converter that receives a reference signal from the processor.

29. (previously presented) A method in accordance with Claim 28 wherein the control circuit includes at least one port, said method further comprising providing an energization state to the at least one port to control a configuration of the at least one connector pin.

30. (currently amended) A method in accordance with ~~Claim 29 wherein the control circuit includes at least one switch assembly including a switch,~~Claim 29 said method further comprising:

utilizing the energization state of the at least one port to control whether ~~a respective at least one switch~~one of the switches is in an open state or a closed state; and

controlling a configuration of the at least one connector pin by utilizing one of the ~~state~~open and closed states of ~~the at least one switch.~~one of the switches.

31. (currently amended) A method in accordance with Claim 30 wherein ~~the at least one switch assembly includes at least~~one of the switches is configured to be one of a Pull-Down switch, a Pull-Up switch, a Discrete High switch, a Discrete Low switch, a positive 15 volt switch, a negative 15 volt switch, a range switch, and a voltage out switch.

32. (previously presented) A control circuit in accordance with Claim 2 wherein said processor is configured to send a message corresponding to the output via an input/output bus.

33. (previously presented) A control circuit in accordance with Claim 32 wherein the message includes one of an absence of a back biased power at said at least one pin and a presence of the back biased power at said at least one pin.

34. (previously presented) A control circuit in accordance with Claim 3 wherein said processor is configured to send a message corresponding to the output via an input/output bus.

35. (previously presented) A control circuit in accordance with Claim 34 wherein the message includes one of an absence of a back biased power at said at least one pin and a presence of the back biased power at said at least one pin.

36. (previously presented) An I/O module in accordance with Claim 7 wherein said processor is configured to send a message corresponding to the output via an input/output bus.

37. (previously presented) An I/O module in accordance with Claim 36 wherein the message includes one of an absence of a back biased power at said at least one pin and a presence of the back biased power at said at least one pin.

38. (previously presented) A PLC in accordance with Claim 13 wherein said processor is configured to send a message corresponding to the output via an input/output bus.

39. (previously presented) A PLC in accordance with Claim 38 wherein the message includes one of an absence of a back biased power at said at least one connector pin and a presence of the back biased power at said at least one connector pin.

40. (previously presented) A method in accordance with Claim 19 further comprising transmitting a message corresponding to the output via an input/output bus.

41. (previously presented) A method in accordance with Claim 40 wherein said transmitting a message comprises sending a message that includes one of an absence of a back biased power at said at least one connector pin and a presence of the back biased power at said at least one connector pin.

42. (previously presented) An I/O module in accordance with Claim 24 wherein said processor is configured to send a message corresponding to the output via an input/output bus.

43. (previously presented) An I/O module in accordance with Claim 42 wherein the message includes one of an absence of a back biased power at said at least one pin and a presence of the back biased power at said at least one pin.

44. (previously presented) An I/O module in accordance with Claim 25 wherein said processor is configured to send a message corresponding to the output via an input/output bus.

45. (previously presented) An I/O module in accordance with Claim 44 wherein the message includes one of an absence of a back biased power at said at least one pin and a presence of the back biased power at said at least one pin.

46. (previously presented) A method in accordance with Claim 28 further comprising transmitting a message corresponding to the output via an input/output bus.

47. (previously presented) A method in accordance with Claim 46 wherein said transmitting a message comprises sending a message that includes one of an absence of a back biased power at said at least one connector pin and a presence of the back biased power at said at least one connector pin.